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April 1, 2002

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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TECHNOLOGY CENTER 2800

Subject: | Serial No. 10/077,093 02/19/02 |
| Subhash Gupta, Pradeep Yelehanka, |
| Vijay Chhagan |
| METHOD TO FORM SELF-ALIGNED, L-SHAPED |
| SIDEWALL SPACERS |
Grp. Art Unit: 2812

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner of Patents and
Trademarks, Washington, D.C. 20231, on April 10, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date SB Ackerman 4/10/02

U.S. Patent 5,891,788 to Fazan et al., "Locus Isolation Technique using High Pressure Oxidation (HIPOX) and Protective Spacers", teaches a process to form local oxidation of silicon (LOCOS) isolations using polysilicon spacers around a masking material.

U.S. Patent 5,661,049 to Lur et al., "Stress Relaxation in Dielectric before Metallization", teaches a process to form sidewalls for transistors.

U.S. Patent 5,013,675 to Shen et al., "Method of Forming and Removing Polysilicon Lightly Doped Drain Spacers", discloses a process to form polysilicon sidewall spacers and to remove them using an etchant.

U.S. Patent 5,899,722 to Huang, "Method of Forming Dual Spacer for Self Aligned Contact Integration", teaches a process to form sidewall spacers of silicon nitride by anisotropically etching a silicon nitride layer.

U.S. Patent 5,498,555 to Lin, "Method of Making LDD with Polysilicon and Dielectric Spacers", discloses processes to form sidewall spacers of: oxide-polysilicon, oxide-polysilicon-oxide, oxide-nitride, and oxide-nitride-oxide.

Sincerely,



Stephen B. Ackerman, Reg. #37761